Optimization of the Silicon Subcell for III-V on Silicon Multijunction Solar Cells: Key Differences with Conventional Silicon Technology

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Abstract. Dual-junction solar cells formed by a GaAsP or GaInP top cell and a silicon (Si) bottom cell seem to be attractive candidates to materialize the long sought-for integration of III-V materials on Si for photovoltaic (PV) applications. Such integration would offer a cost breakthrough for PV technology, unifying the low cost of Si and the efficiency potential of III-V multijunction solar cells. The optimization of the Si solar cells properties in flat-plate PV technology is well- known; nevertheless, it has been proven that the behavior of Si substrates is different when processed in an MOVPE reactor In this study, we analyze several factors influencing the bottom subcell performance, namely, 1) the emitter formation as a result of phosphorus diffusion; 2) the passivation quality provided by the GaP nucleation layer; and 3) the process impact on the bottom subcell PV properties.

Keywords: III-V on Silicon, MOVPE, heteroepitaxy, MJSC, bottom subcell.
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INTRODUCTION

Multijunction solar cell (MJSC) architectures offer a tremendous potential for achieving very high photovoltaic (PV) conversion efficiencies. State-of-the-art III-V MJSC designs are based on a substrate material (namely germanium), which is both costly and rare. These factors have given rise to an active quest for alternative substrates, where silicon (Si) emerges as a natural choice as a result of its abundance and low cost. One of the most successful approaches is based on the use of a GaP nucleation layer to achieve a defect-free III-V template on Si [1-3], where graded buffers can be grown to form a GaAsP/Si or a GaInP/Si dual junction solar cell.

The growth of this structure involves several challenges due to the difficulty for obtaining a defect-free structure. However, the optimization of the bottom cell will be crucial to obtain a high quality solar cell since the minority carrier parameters of the bottom cell base will determine the PV performance of the bottom sub-cell in the tandem stack [4]. The optimization of the Si substrate in flat-plate PV technology is well- known; nevertheless, it has been proven that the behavior of the Si substrates is different when processed in an MOVPE (MetalOrganic Vapor Phase Epitaxy) environment. This paper reviews several key features for the design and optimization of the bottom subcell; particularly: 1) the emitter formation as a result of the phosphorus (P) diffusion that takes place during the MOVPE process; 2) the passivation quality provided by the GaP nucleation layer to the emitter of the Si subcell and 3) the process impact on the bottom cell minority carrier lifetime.

EMITTER FORMATION

When manufacturing a MJSC on Si, one of the first processes to be addressed is the formation of the emitter of the Si subcell. P diffusion in crystalline Si is a well-known phenomenon which has been thoroughly studied in the past 40 years [5]. However, the formation of the n++ emitter in the Si subcell in a MOVPE environment is a complex process somewhat dissimilar to the traditional diffusion step in conventional PV technology due to the difference of the working conditions.

Essentially, two alternatives exist for this process: 1) the epitaxially growth of the emitter, which implies the homoepitaxial growth of n-type Si on the p-type wafer; 2) mimicking what is done on III-V on Ge MJSC technology; the Si emitter subcell is, then, formed by diffusion of a group-V element. In a MOVPE reactor, as a result the P surface coverage at the elevated temperatures, diffusion of P into the wafer takes place. Furthermore, the thermal load associated with the rest of the structure, may contribute to the P drive-in process. The use of homoepitaxial growth has demonstrated to be a beneficial factor in the production of high quality GaP layers [2,3], though introduces an additional degree of complexity in the epitaxial process. However, several groups have also reported high quality GaP layers without homoepitaxial Si buffers [1]. Accordingly, we will focus on this strategy and consider the formation of the emitter from diffusion as is the case in conventional MJSC based on Ge.

In order to quantify the emitter depth, samples (treated under different diffusion conditions) were measured using the ECV and SIMS techniques (Fig.

1). The usual profile obtained in the conventional PV technology has been used as a reference. This profile considers the various mechanisms (vacancy-mediated diffusion at high P concentrations and an interstitially driven diffusion at lower P concentrations) that give rise to the typical kink-and-tail profile [5]. Furthermore, an additional theoretical profile, which considers an enhanced role of self interstitials, has been also included.

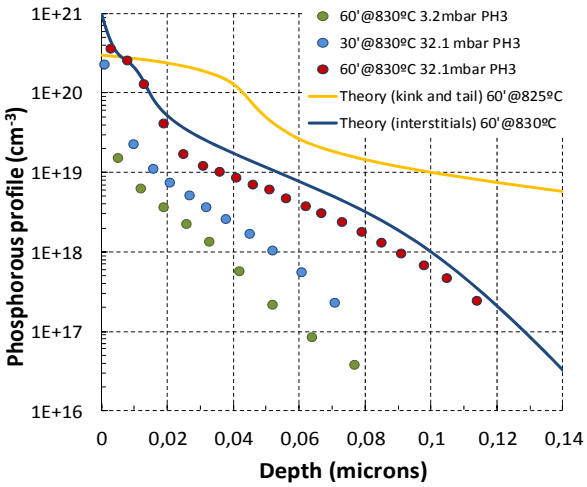

FIGURE 1. ECV Profiles measured on Si wafers annealed at 830ºC under different flows of PH_3. The expected theoretical profiles –considering two different diffusion mechanisms- are included as solid lines.

Leaving aside possible deviations in the real surface temperature of the wafer, there is an evident disagreement between the modeling of conventional diffusion profiles and the experimental ones as measured by ECV in MOVPE treated samples, which follows better the interstitially dominated diffusion profile. As we can see in figure 1, the P surface coverage (and the emitter depth) can be controlled by temperature and PH_3 partial pressure.

ROLE OF THE INTERFACES

Another aspect being evaluated is the quality of the passivation provided by the GaP nucleation layer to the emitter of the Si subcell. Emitter passivation is an important issue in conventional Si solar cell technology, where surfaces are passivated using a stable nitride layer, leading to low surface recombination velocity. In this technology, the degradation of surface morphology at the nanoscale is not an issue. However, in the integration of III-V compounds on Si for MJSC applications, Si substrates will be passivated with a GaP nucleation layer grown epitaxially by MOVPE. Two requirements are needed to guarantee an optimal heteroepitaxy: 1) High quality surface morphology for subsequent III-V epitaxy and 2) an optimized nucleation routine to avoid the 3D growth and structural defects formation.

Substrate Morphology

A side effect of the diffusion process is the degradation of the substrate surface morphology. It has been described that Si (100) surfaces exposure to PH_3 may result in surface roughening due to Si hydration and subsequent dimmer displacement [6]. Roughening and foreign species typically generate antiphase disorder and other crystallographic defects in the GaP nucleation layer, which grows exhibiting poor morphology and thus limiting the quality of the active layers of the device. Consequently, the optimum diffusion conditions for the formation of the bottom subcell emitter have to be attained without degrading the morphology of the substrate.

The effect of different thermal treatments has been studied by characterizing wafers using Atomic Force Microscopy (AFM). This study is sumarised in figure 2, where an as-received wafer has been also included for comparison (Fig. 2a).

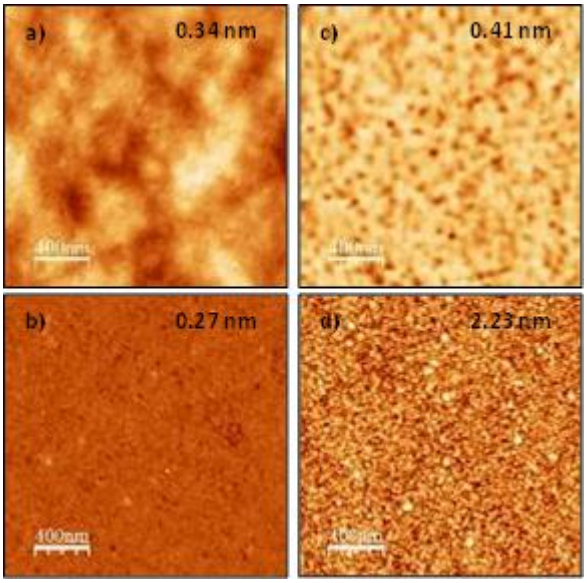

FIGURE 2. AFM topography scans of Si wafers annealed at 830ºC for 60 min. under different PH_3 partial pressures (a) As received wafer; (b) No PH_3; (c) 3.2 mbar; (d) 32.1 mbar of PH_3. RMS roughness for each case is indicated on the top-right corner of each scan.

As shown by the random presence of dark dots in all scans, all samples present pits (holes), which were not present in the AFM scans of as received wafers. A clear change in surface RMS roughness can be appreciated in the samples exposed to PH_3 (table 1). Surface skewness –which should be zero for a morphology consisting of evenly distributed peaks and valleys of homogeneous heights– is negative in the three cases, indicating that the samples present larger valleys than peaks. Surface kurtosis also increases with PH_3 anneal suggesting a transition to a spikier surface.

After the formation of the emitter, surface morphology has to be greatly improved. Therefore,

wafers have to be submitted to a thermal process to ensure a high quality surface for epitaxial growth and therefore to attain a good GaP passivation [7].

TABLE 1. Roughness parameters of the AFM scans included in Fig 2.

Treatment	RMS roughness	Surface skewness	Surface kurtosis
As received	0.34 nm	0.05	3.07
No PH_3	0.27 nm	-0.30	7.00
3.2 mbar PH_3	0.41 nm	-0.95	4.22
32.1 mbar PH_3	2.23 nm	-0.05	3.02

GaP Nucleation

In order to assess the suitability of the Si surface for subsequent III-V growth, GaP nucleation layers were grown -on samples annealed at high temperature under hydrogen- following different nucleation routines.

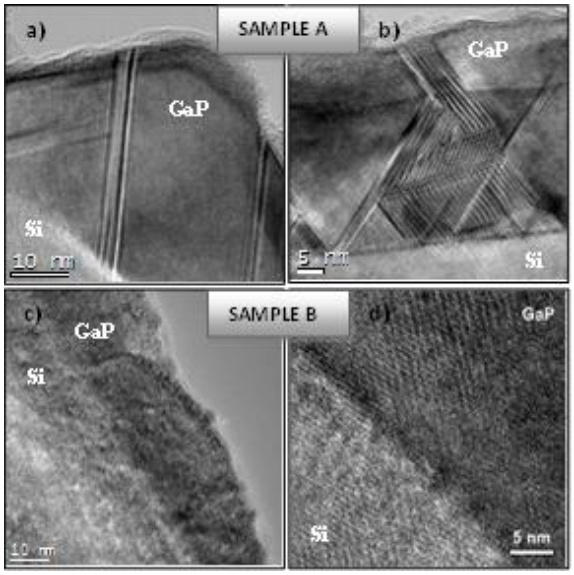

FIGURE 3. TEM images of a GaP layer grown on silicon following a low temperature nucleation routine (sample A) and a high temperature nucleation routine (sample B).

Figure 3 shows STEM micrograph of this GaP layer which has been grown following two different routines. Sample A (Fig. 3a, 3b) –low temperature nucleation routine- presents an island-type growth, where defects were originated at the interface and were propagated until the surface. Sample B (Fig. 3c, 3d), on the contrary, has followed a high temperature nucleation routine. Although its morphology still has to be greatly improved, no stacking faults were found inside the GaP layer and only a few dislocations were detected in the sample. Figure 3d reveals an interface of very good crystallographic quality.

PROCESS IMPACT ON LIFETIME

The bottom cell base minority carrier parameters determine the PV performance of the bottom sub-cell in the tandem stack [4]. From conventional Si PV technology it is well documented that the impurities that are contained in the wafers can eventually be activated during a high temperature step (e.g. formation of B-O pairs) [8]. On the contrary, the P diffused into the Si (forming the emitter) may act as a gettering center, extracting metal impurities from the bulk material, and hence increasing the base layer bulk minority carrier lifetime [9]. The wafer exposure to an environment where several group-III and group-V species coexist in the presence of high temperatures and organic radicals may also have an impact in the concentration of SRH centers.

The impact of different processes carried out in a MOVPE reactor on the minority carrier lifetime of Czochralski grown Si have been evaluated. Samples were then characterized using Photoconductance Lifetime Tester which allows to measure the bulk minority carrier lifetime (Fig. 4). They were surface passivated using a Quinhydrone:Methanol solution.

After the formation of the emitter –for the higher phosphine partial pressure and temperature–, an important improvement of lifetime, with respect to as-received wafer, was observed. However, when lower phosphine partial pressures were used to form the emitter, an important reduction of the lifetime was observed, reaching values even lower than the detection limit of the equipment for the most extreme conditions (in the absence of PH_3). This means that the gettering effect of phosphorous is optimum for a given partial pressure and temperature. Annealing at different conditions implies either a stronger dissolution or in-diffusion of impurities (which becomes a dominant phenomenon), or the formation of structural defects, leading to a significant reduction of the lifetime. There are three different reasons for explaining this behavior: 1) dissolution of internal metallic impurities, 2) activation of B-O pairs and 3) introduction on external impurities. To clarify this issue, the last experiment (annealing in hydrogen, with no PH_3) was used as a reference, since its conditions causes the most extreme reduction of lifetime (table 2). Firstly and with the aim of proving that the lifetime reduction is not related with a poor wafer quality, experiments were repeated on wafers from a different supplier. The same results were obtained. Furthermore, in order to find out if the activation of B-O pairs during the MOVPE process was the reason for this behavior, Gallium doped Czochralski Silicon wafers were also used. Since the same behavior was once again observed, the lifetime degradation should be related with the introduction of some contaminants, either during the pretreatment

of wafers (before being loaded into the reactor), or during the MOVPE process.

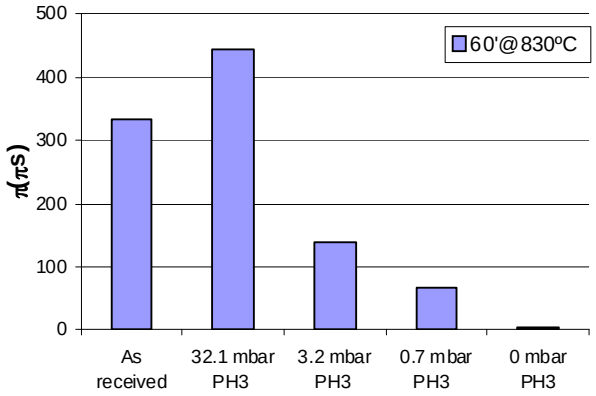

FIGURE 4. Minority carrier bulk lifetime for P-diffused wafers after removing the diffused emitter. Wafers were heated during 60 minutes for different phosphine partial pressures. Average bulk lifetime of as-received wafers has been includedfor comparison.

TABLE 2. Lifetime values for wafers annealed in hydrogen for different times. An as received sample was included in all the cases for comparison.

Treatment	Si:B Supplier A	Si:B Supplier B	Si:Ga Supplier C
As recevied	390	215	250
60'@830ºC	<10	<10	<10
120'@830ºC	<10	<10	<10

SUMMARY AND CONCLUSIONS

Dual-junction solar cells formed by a GaAsP or GaInP top cell and a Si bottom cell seem to be excellent candidates for the integration of III-V materials on Si. Although the optimization of Si solar cells in flat-plate PV technology is well known; the behavior of the Si substrate is different when it is processed in an MOVPE environment. Several factors impacting the optimization of the bottom subcell have been analyzed. The formation of the emitter by P diffusion will be determined by the initial steps at high temperature. Since the formation of the emitter leads to an important degradation of the surface, wafers have to be submitted to a thermal process (before the MOVPE growth) to ensure a high quality surface for epitaxial growth. Furthermore, different nucleation routines have been carried out to study the quality passivation of GaP. Although the morphology has to be still improved, a high crystalline quality has been obtained. Finally, the minority carrier lifetime of the bottom subcell base has been measured for wafers that have submitted to different diffusion conditions.

The gettering effect of P is optimum for a given partial pressure and temperature, while annealing at different conditions implies an important reduction on lifetime, reaching minimum values when no phosphine is present. Different hypotheses have been considered to explain this behavior. The introduction of contaminants (either during the pretreatment of wafers or during the MOVPE process) is the most likely option.

Therefore, a compromise between the three points above mentioned (i.e the formation of a bottom subcell with a suitable emitter, an optimal surface morphology and with high PV quality) is required to obtain an optimal bottom subcell.

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